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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/977,699	10/16/2001	Thomas N. Indermaur	10007795-1	3755

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EXAMINER	
DIMYAN, MAGID Y	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/977,699	INDERMAUR, THOMAS N.	
	Examiner	Art Unit	
	Magid Y Dimyan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2004 and 19 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,8-14,16,17 and 19-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,8-14,16,17 and 19-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 May 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Acknowledgement

1. This is with reference to the Amendments to the Claims, and Remarks, both filed September 30, 2004 and to the Remarks filed October 19, 2004. It is acknowledged that the Applicant amended claims 1, 8, 10, 16 and 19, and cancelled claims 2, 7, 15 and 18 without introducing new matter. It is also acknowledged that the Applicant has amended the claim language to overcome the claim objections cited in the previous Office Action. However, the Applicant's arguments were not persuasive to overcome the claim rejections. The pending claims are therefore rejected for the reasons given below. Claims 1, 3 – 6, 8 – 9, 11 – 14, 17 – 17 and 19 –23 remain pending in this application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3 – 6, 8 – 9, 10 – 14, 16 – 17 and 19 - 23 rejected under 35 U.S.C. 103(a) as being unpatentable over Pub. No. US 2002/0046386 to Skoll et al (hereinafter, Skoll), in view of U.S. Patent No. 6,263, 480 to Bartels et al. (hereinafter, "Bartels").

4. Referring to claim 1, Skoll recites the elements claimed herein of determining the location of a short in a circuit that includes (a) running a connectivity extraction (see page 1, paragraphs 3 and 6); (b) determining and locating a short in the circuit using the schematic (see page 3, paragraph 32 and page 8, paragraphs105 – 106); (c) making a copy of the artwork (see column 6, paragraphs 73 – 75); and (d) comparing artwork with the schematic (see Figs. 15 A, 15B and page 8, paragraph 107). However, Skoll does not teach the added element of obtaining a shortest path between conflicting labels in the circuit wherein the shortest path contains the short in the circuit. On the other hand, Bartels cites a methodology for the efficient tracing of shorts as the shortest path in hierarchical VLSI devices (see Abstract; col. 2, lines 3 – 61). Since, as stated by Bartels (col. 2, lines 27 – 30), finding the shortest path that contains the short in a circuit is necessary to trace shorts efficiently with respect to time and storage requirements in large hierarchical designs, it would therefore be obvious to a person of ordinary skill in the art at the time of the invention to combine the teachings of Skoll and Bartels to obtain the same claimed invention.

5. As for claims 3 and 4, see (4) above, as well as Skoll - Figs. 15A and 15 B; and page 8, paragraphs 104 – 107, which disclose how to evaluate the connectivity text file of the schematic and obtaining the electrical connection information, as claimed herein.

6. As per claim 5, see Skoll - Fig. 12; and page 7, paragraphs 83 – 86, which cite how the signal names are labeled, as claimed herein.

7. Referring to claim 6, see above, as well as page 6, paragraphs 73 - 75, which cite how an edit and a copy of the artwork can be generated before running the tool, as claimed herein.

8. Pursuant to claim 8, see Skoll – page 3, paragraph 26 which teach how the artwork can be modified as claimed.

9. As to claim 9, see Skoll – page 3, paragraphs 26 – 30 which show how extraction can be performed on a copy of the artwork, as claimed.

10. Referring to claim 10, Skoll teaches the elements of: (a) examining a schematic (see Skoll - Fig. 4; and page 5, paragraph 59); and (b) creating a copy of the artwork of the circuit (see Skoll - column 6, paragraphs 73 – 75). But Skoll does not teach the element of using a short locator tool to obtain the shortest path between conflicting labels in a circuit. However, as indicated in (4) above,

Bartels cites a methodology for the efficient tracing of shorts as the shortest path in hierarchical VLSI devices (see Abstract; col. 2, lines 3 – 61). Since, as stated by Bartels (col. 2, lines 27 – 30), finding the shortest path that contains the short in a circuit is necessary to trace shorts efficiently with respect to time and storage requirements in large hierarchical designs, it would therefore be obvious to a person of ordinary skill in the art at the time of the invention to combine the teachings of Skoll and Bartels to obtain the same claimed invention.

11. Claims 11 – 14 contain the same limitations as claims 3 – 5, respectively, and thus the same rejections apply.

12. Claims16 and 17 contain the same limitations as claims 8 and 9, respectively, and thus the same rejections also apply.

13. Referring to claim 19, Skoll teaches the elements of a method comprising: (a) running a connectivity extract tool on an artwork to determine with a short exists in a circuit (see (4) above; paragraphs 32 and 105 – 107); (b) if a short exists determining it's location evaluating a schematic text file associated with the circuit to identify each connection (Figs. 15A and 15B), creating a copy of the artwork (see above; and paragraphs 73 – 75), inferring and renaming labels associated with identified connections (paragraphs 83 – 86). Although Skoll also teaches running a connectivity tool (see (4) above), Skoll does not teach identifying the shortest electrical path when a short circuit exists. However, as

recited in (4) above, Bartels discloses a methodology for the efficient tracing of shorts as the shortest path in hierarchical VLSI devices (see Abstract; col. 2, lines 3 – 61). Since, as stated by Bartels (col. 2, lines 27 – 30), finding the shortest path that contains the short in a circuit is necessary to trace shorts efficiently with respect to time and storage requirements in large hierarchical designs, it would therefore be obvious to a person of ordinary skill in the art at the time of the invention to combine the teachings of Skoll and Bartels to obtain the same claimed invention.

14. As per claims 20 – 23 see (4) and (13) above, as well as Skoll - paragraphs 101 – 107, which also teach how short circuits can be obtained by isolating portions of the artwork on a workstation that contain errors, modified when errors (i.e., short circuits) are found, and rerunning the connectivity tool on the modified copy of the artwork for verification.

Response to Arguments

15. Applicant's arguments with respect to claims 1, 3 – 6, 8 – 9, 10 – 14, 16 – 17 and 19 - 23 have been considered but are moot in view of the new ground(s) of rejection, as well as for providing the motivation for establishing a prima facie case of obviousness as cited above.

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y Dimyan whose telephone number is (571) 272-1889. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272-1907.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Magid Y Dimyan
Examiner
Art Unit 2825

myd
14 December 2004

MYD

A. M. Thompson
Primary Examiner
Technology Center Z800